EAST SEARCH

9/9/2006

L#	Hits	Search String	Databases
S1	12	very long instruction word with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S2	77	very long instruction word same simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S3	1929	very long instruction word with processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S4	1951	S2 or S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S5	55	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S6	13	S4 and (simulat$3 with ((group or set or plurality) near2 instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S7	408	S4 and simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S9	59	S7 and (simulat$3 with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S10	32	S7 and (simulat$3 with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S12	4	S7 and (generat$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S27	6	very long instruction word with processor with resource	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S11	2	S7 and (simulat$3 with cycle-by-cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S28	17	S7 and (stor$3 with "register set")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S13	0	S7 and (generat$3 with instuction with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S14	2	S7 and (display$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S33	4	S7 and ((count$3 or number) with (execution near2 cycle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S35	3	S7 and (cancel$3 with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S16	1	S7 and (simulat$3 with stop with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S17	1	S7 and (break with condition with stop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S18	50	S7 and (simulat$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S19	12	S7 and (simulat$3 with (simultaneous$2 or concurrent$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S20	2	S7 and (display$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S21	102	S7 and (pipeline with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S22	43	S7 and (pipeline with stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S23	9	S7 and (simulat$3 with step with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S24	10	S7 and (step with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S47	12	S44 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S25	7	S7 and (step with execution with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S26	2	S7 and (step with execution with display$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S29	14	S7 and ((reconstruct$3 or creat$3 or generat$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S8	2	S7 and (simulat$3 with instruction-by-instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S30	102	S7 and ((sav$3 or stor$3) with (memory near2 (data or writing)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S31	3	S7 and (break with condition with determin$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S32	10	S7 and ((updat$3 or chang$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S36	25	S7 and (delay$3 with (cycle or insruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S37	137	S7 and (updat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S34	3	S7 and (cancel$3 with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S39	218	S7 and ((updat$3 or delay) with (information or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S38	4	S7 and (output near2 dependency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S41	162	S1 or S2 or S5 or S6 or S8 or S9 or S10 or S11 or S12 or S14 or S15 or S16 or S17 or S18 o	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S40	183	S7 and ((updat$3 or delay) with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S42	304	S21 or S30 or S37 or S40 or S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S43	142	S41 and S42	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S44	162	S41 or S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S45	13	S44 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S46	0	S7 and (simulat$3 with instruction-based)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S15	3	S7 and (break with condition with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S61	3	S54 and (break with condition with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S68	43	S54 and (pipeline with stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S62	1	S54 and (simulat$3 with stop with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S60	2	S54 and (display$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S51	1952	S49 or S50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S64	50	S54 and (simulat$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S76	102	S54 and ((sav$3 or stor$3) with (memory near2 (data or writing)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S58	2	S54 and (simulat$3 with cycle-by-cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S56	59	S54 and (simulat$3 with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S66	2	S54 and (display$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S52	55	S49 and S50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S48	12	very long instruction word with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S54	408	S51 and simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S53	13	S51 and (simulat$3 with ((group or set or plurality) near2 instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S55	2	S54 and (simulat$3 with instruction-by-instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S59	4	S54 and (generat$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S49	77	very long instruction word same simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S50	1930	very long instruction word with processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S57	32	S54 and (simulat$3 with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S63	1	S54 and (break with condition with stop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S70	10	S54 and (step with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S65	12	S54 and (simulat$3 with (simultaneous$2 or concurrent$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S67	102	S54 and (pipeline with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S93	5	S51 and (pipeline with cycle with (simulat$3 or debug$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S71	7	S54 and (step with execution with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S69	9	S54 and (simulat$3 with step with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S72	2	S54 and (step with execution with display$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S103	28	S101 or S102	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S73	6	very long instruction word with processor with resource	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S74	17	S54 and (stor$3 with "register set")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S90	162	S87 or S89	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S94	8	S51 and (pipeline with instruction with (simulat$3 or debug$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S75	14	S54 and ((reconstruct$3 or creat$3 or generat$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S101	28	S99 or S100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S77	3	S54 and (break with condition with determin$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S78	10	S54 and ((updat$3 or chang$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S79	4	S54 and ((count$3 or number) with (execution near2 cycle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S82	25	S54 and (delay$3 with (cycle or insruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S80	3	S54 and (cancel$3 with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S83	137	S54 and (updat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S81	3	S54 and (cancel$3 with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S87	162	S48 or S49 or S52 or S53 or S55 or S56 or S57 or S58 or S59 or S60 or S61 or S62 or S63 c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S88	304	S67 or S76 or S83 or S86 or S85	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S84	4	S54 and (output near2 dependency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S85	218	S54 and ((updat$3 or delay) with (information or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S86	183	S54 and ((updat$3 or delay) with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S89	142	S87 and S88	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S95	12	S51 and (((group or multiple or plurality) near2 instruction) with (simulat$3 or debug$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S91	325	S51 and (pipeline with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S92	419	S51 and (pipeline with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S96	18	S93 or S94 or S95	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S98	18	S96 or S97	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S97	17	S96 and (S87 or S88)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S99	5	S91 and (cycle with debug$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S100	28	S92 and (instruction with debug$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S102	11	S101 and (S87 or S88)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

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Results of search set S91:

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20060174059 A1	Speculative data loading using circular addressing or simulated circular addressing	20060803	711/110	
US 20060150170 A1	Methods and apparatus for automated generation of abbreviated instruction set and configur	20060706	717/158	
US 20060107158 A1	Functional coverage driven test generation for validation of pipelined processors	20060518	714/741	
US 20060095750 A1	Processes, circuits, devices, and systems for branch prediction and other processor improver	20060504	712/240	
US 20060095745 A1	Processes, circuits, devices, and systems for branch prediction and other processor improver	20060504	712/238	
US 20060095716 A1	Super-reconfigurable fabric architecture (SURFA): a multi-FPGA parallel processing architect	20060504	712/24	
US 20060075285 A1	Fault processing for direct memory access address translation	20060406	714/5	
US 20060067436 A1	Metacores: design and optimization techniques	20060330	375/341	
US 20060047776 A1	Automated failover in a cluster of geographically dispersed server nodes using data replicatio	20060302	709/217	
US 20060015855 A1	Systems and methods for replacing NOP instructions in a first program with instructions of a s	20060119	717/136	
US 20050289259 A1	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20051229	710/72	
US 20050262510 A1	Multi-threaded processing design in architecture with multiple co-processors	20051124	718/105	
US 20050223253 A1	Methods and apparatus for power control in a scalable array of processor elements	20051006	713/322	
US 20050216702 A1	Dual-processor complex domain floating-point DSP system on chip	20050929	712/35	
US 20050189976 A1	Enhanced negative constraint calculation for event driven simulations	20050901	327/175	
US 20050182916 A1	Processor and compiler	20050818	712/24	
US 20050172050 A1	Methods and apparatus for providing data transfer control	20050804	710/22	
US 20050166039 A1	Programmable event driven yield mechanism which may activate other threads	20050728	712/227	
US 20050162456 A1	Printer with capacitive printer cartridge data reader	20050728	347/19	
US 20050151777 A1	Integrated circuit with tamper detection circuit	20050714	347/19	
US 20050149697 A1	Mechanism to exploit synchronization overhead to improve multithreaded performance	20050707	712/214	
US 20050149693 A1	Methods and apparatus for dual-use coprocessing/debug interface	20050707	712/34	
US 20050086653 A1	Compiler apparatus	20050421	717/151	
US 20050086040 A1	System incorporating physics processing unit	20050421	703/22	

US 20050075849 A1	Physics processing unit	20050407	703/2
US 20050075154 A1	Method for providing physics simulation data	20050407	463/1
US 20050055389 A1	Method, apparatus and instructions for parallel data conversions	20050310	708/204
US 20050038936 A1	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20050217	710/22
US 20050027973 A1	Methods and apparatus for scalable array processor interrupt detection and response	20050203	712/233
US 20050010743 A1	Multiple-thread processor for threaded software applications	20050113	712/10
US 20040268051 A1	Program-directed cache prefetching for media processors	20041230	711/137
US 20040218048 A1	Image processing apparatus for applying effects to a stored image	20041104	348/207.2
US 20040172524 A1	Method, apparatus and compiler for predicting indirect branch target addresses	20040902	712/239
US 20040163083 A1	Programmable event driven yield mechanism which may activate other threads	20040819	718/102
US 20040162925 A1	Methods and apparatus for providing data transfer control	20040819	710/22
US 20040154002 A1	System & method of linking separately compiled simulations	20040805	717/135
US 20040153634 A1	Methods and apparatus for providing context switching between software tasks with reconfigu	20040805	712/228
US 20040117172 A1	Simulation apparatus, method and program	20040617	703/22
US 20040103193 A1	Response time and resource consumption management in a distributed network environment	20040527	709/224
US 20040093484 A1	Methods and apparatus for establishing port priority functions in a VLIW processor	20040513	712/216
US 20040088462 A1	Interrupt control apparatus and method	20040506	710/261
US 20040078674 A1	Methods and apparatus for generating functional test programs by traversing a finite state mc	20040422	714/33
US 20040068701 A1	Boosting simulation performance by dynamically customizing segmented object codes based	20040408	716/4
US 20040065738 A1	Data distribution mechanism in the form of ink dots on cards	20040408	235/454
US 20040060018 A1	Defect tracking by utilizing real-time counters in network computing environments	20040325	716/4
US 20040054871 A1	Methods and apparatus for initiating and resynchronizing multi-cycle SIMD instructions	20040318	712/22
US 20040025073 A1	Method for transforming behavioral architectural and verification specifications into cycle-bas	20040205	713/400
US 20040015931 A1	Methods and apparatus for automated generation of abbreviated instruction set and configur	20040122	717/158
US 20040008327 A1	Image printing apparatus including a microcontroller	20040115	355/18
US 20040008262 A1	Utilization of color transformation effects in photographs	20040115	348/207.2
US 20040008261 A1	Print roll for use in a camera imaging system	20040115	348/207.2
US 20030226120 A1	Metacores: design and optimization techniques	20031204	716/1
US 20030204819 A1	Method of generating development environment for developing system LSI and medium whic	20031030	716/1
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002	717/141
US 20030182539 A1	Storing execution results of mispredicted paths in a superscalar computer processor	20030925	712/225
US 20030171907 A1	Methods and Apparatus for Optimizing Applications on Configurable Processors	20030911	703/14
US 20030154349 A1	Program-directed cache prefetching for media processors	20030814	711/137
US 20030079065 A1	Methods and apparatus for providing data transfer control	20030424	710/22
US 20030040898 A1	Method and apparatus for simulation processor	20030227	703/21
US 20030040896 A1	Method and apparatus for cycle-based computation	20030227	703/13
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
US 20030036893 A1	Method and apparatus for simulating transparent latches	20030220	703/16
US 20020165709 A1	Methods and apparatus for efficient vocoder implementations	20021107	704/201
US 20020138712 A1	Data processing device with instruction translator and memory interface device	20020926	712/205
US 20020133784 A1	Automatic design of VLIW processors	20020919	716/1
US 20020129227 A1	Processor having priority changing function according to threads	20020912	712/228
US 20020124155 A1	Processor architecture	20020905	712/218
US 20020124012 A1	Compiler for multiple processor and distributed memory architectures	20020905	707/200
US 20020120914 A1	Automatic design of VLIW processors	20020829	716/17
US 20020078320 A1	Methods and apparatus for instruction addressing in indirect VLIW processors	20020620	712/24
US 20020042897 A1	Method and system for distributed testing of electronic devices	20020411	714/718
US 20020019910 A1	Methods and apparatus for indirect VLIW memory allocation	20020214	711/125

US 20020010814 A1	Methods and apparatus for providing data transfer control	20020124	710/22
US 20020004916 A1	Methods and apparatus for power control in a scalable array of processor elements	20020110	713/322
US 20020002640 A1	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20020103	710/22
US 20020002639 A1	Methods and apparatus for loading a very long instruction word memory	20020103	710/22
US 20010049763 A1	Methods and apparatus for scalable array processor interrupt detection and response	20011206	710/264
US 20010032305 A1	Methods and apparatus for dual-use coprocessing/debug interface	20011018	712/34
US 20010032067 A1	METHOD AND SYSTEM FOR DETERMINING OPTIMAL DELAY ALLOCATION TO DATAPA	20011018	703/14
US 20010027499 A1	Methods and apparatus for providing direct memory access control	20011004	710/26
US 20010025363 A1	Designer configurable multi-processor system	20010927	716/1
US 7084951 B2	Combined media- and ink-supply cartridge	20060801	355/18
US 7080365 B2	Method and apparatus for simulation system compiler	20060718	717/146
US 7076416 B2	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20060711	703/15
US 7065723 B2	Defect tracking by utilizing real-time counters in network computing environments	20060620	716/4
US 7062735 B2	Clock edge value calculation in hardware simulation	20060613	716/6
US 7051309 B1	Implementation of fast data processing with mixed-signal and purely digital 3D-flow processin	20060523	716/10
US 7051303 B1	Method and apparatus for detection and isolation during large scale circuit verification	20060523	716/4
US 7050143 B1	Camera system with computer language interpreter	20060523	355/18
US 7043596 B2	Method and apparatus for simulation processor	20060509	710/317
US 7036114 B2	Method and apparatus for cycle-based computation	20060425	717/149
US 7028286 B2	Methods and apparatus for automated generation of abbreviated instruction set and configur	20060411	717/106
US 7024540 B2	Methods and apparatus for establishing port priority functions in a VLIW processor	20060404	712/200
US 7017126 B2	Metacores: design and optimization techniques	20060321	716/1
US 7003450 B2	Methods and apparatus for efficient vocoder implementations	20060221	704/201
US 6986020 B2	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20060110	712/10
US 6978460 B2	Processor having priority changing function according to threads	20051220	718/103
US 6961843 B2	Method frame storage using multiple memory circuits	20051101	712/208
US 6944683 B2	Methods and apparatus for providing data transfer control	20050913	710/22
US 6892328 B2	Method and system for distributed testing of electronic devices	20050510	714/42
US 6889317 B2	Processor architecture	20050503	712/218
US 6883088 B1	Methods and apparatus for loading a very long instruction word memory	20050419	712/215
US 6871298 B1	Method and apparatus that simulates the execution of paralled instructions in processor funct	20050322	714/33
US 6868490 B1	Methods and apparatus for providing context switching between software tasks with reconfigu	20050315	712/15
US 6842811 B2	Methods and apparatus for scalable array processor interrupt detection and response	20050111	710/260
US 6834295 B2	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20041221	709/212
US 6826522 B1	Methods and apparatus for improved efficiency in pipeline simulation and emulation	20041130	703/22
US 6823505 B1	Processor with programmable addressing modes	20041123	717/140
US 6775810 B2	Boosting simulation performance by dynamically customizing segmented object codes based	20040810	716/4
US 6772106 B1	Retargetable computer design system	20040803	703/21
US 6754687 B1	Methods and apparatus for efficient cosine transform implementations	20040622	708/402
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US 6735690 B1	Specifying different type generalized event and action pair in a processor	20040511	712/244
US 6721822 B2	Methods and apparatus for providing data transfer control	20040413	710/33
US 6704857 B2	Methods and apparatus for loading a very long instruction word memory	20040309	712/215
US 6694385 B1	Configuration bus reconfigurable/reprogrammable interface for expanded direct memory acc	20040217	710/8
US 6681280 B1	Interrupt control apparatus and method separately holding respective operation information o	20040120	710/261
US 6658655 B1	Method of executing an interpreter program	20031202	717/139
US 6654870 B1	Methods and apparatus for establishing port priority functions in a VLIW processor	20031125	712/24
US 6651222 B2	Automatic design of VLIW processors	20031118	716/1

US 6622234 B1	Methods and apparatus for initiating and resynchronizing multi-cycle SIMD instructions	20030916	712/22
US 6606721 B1	Method and apparatus that tracks processor resources in a dynamic pseudo-random test pro	20030812	714/728
US 6604067 B1	Rapid design of memory systems using dilation modeling	20030805	703/21
US 6581187 B2	Automatic design of VLIW processors	20030617	716/1
US 6581152 B2	Methods and apparatus for instruction addressing in indirect VLIW processors	20030617	712/24
US 6507947 B1	Programmatic synthesis of processor element arrays	20030114	717/160
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US 6453367 B2	Methods and apparatus for providing direct memory access control	20020917	710/26
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US 6260082 B1	Methods and apparatus for providing data transfer control	20010710	710/22
US 6256683 B1	Methods and apparatus for providing direct memory access control	20010703	710/26
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